Recent Developments in HDI Substrate Electrical Test Engineering

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Introduction

As the trend in the electronics industry continues to make smarter, lighter, smaller, and faster products, new technological developments toward miniature, inexpensive and robust printed wiring boards are needed to be introduced. High density interconnects packages such as FCBGA, FCPGA, MCM, CSP, COB, have become major products aiming to cost-effective surface mounting requirements for both low and high pin counts as well as low and high power dissipation applications. While the fabrication process of HDI packages encounters with several challenges due to shrinking of signal patterns and via dimensions, stringent requirements in the electrical test engineering of such packages are also obvious.

In this report, we have analyzed dominant issues in electrical characterization of HDI substrates and presented their solutions based on advanced and automated electrical measurement techniques.

Quality Issues in the HDI Packages

Power dissipation of high-speed microprocessors manufactured by state-of-the-art semiconductor technology has been increased up to ten folds compared to those CPUs produced a decade ago. A very high current and stable power must be delivered to CPU in order to perform its complex functions of the system. Therefore, it is crucial to have flawless flow of current in the power distribution paths. Defects in the interconnects will lead to reliability issues of the CPUs.

A. Incomplete vias

The imperfect metalization and or poor adhesion inside the microvia barrel is one of the most common failure mode in the HDI substrates. Such incomplete vias, as illustrated in Figure 1, have considerably increased pattern resistances although detection of such small resistance increment is beyond the capability of conventional open short electrical testers.

In fact, the resistance increment in the incomplete vias by be as large as 10 times or more compared their correct values. Whilst the nominal resistance value between the two net ends, for example, is 20 milliohms in a working condition, it is not uncommon to see an actual resistance increased to be 200 milliohms in case that an incomplete via is included in the path.

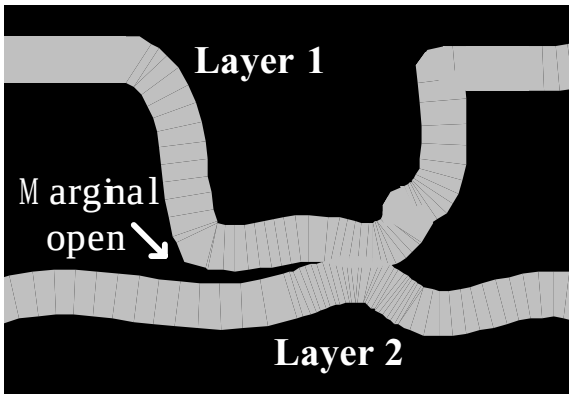

Figure 1 - Cross Section of an Incomplete Via

Suppose a CPU consumes 1A of current from a 1.6V supply as shown in Figure 2, the voltage drop across the pattern resistance will be well over 10% of supply voltage provided that the actual resistance is 200 milliohms, instead of the nominal 20 milliohms.

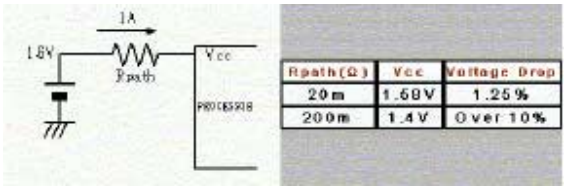

Figure 2 - Examples of Voltage Drops

In addition to this significant potential drop, an incomplete vias also increases the inductance along the signal path, and thereby deteriorates the important ac characteristics of the substrate. Therefore, the quality of microvias on HDI substrates should be inspected prior to shipping especially for a high speed and high power applications.

B. Microshorts

A microshort is defined as a shorted electrical path between the nominally isolated patterns, which can be easily broken by applying high enough electrical

voltage. These types of undesirable short circuits are formed due to migration of conductive ions in the dielectric materials as shown in Figure 3.

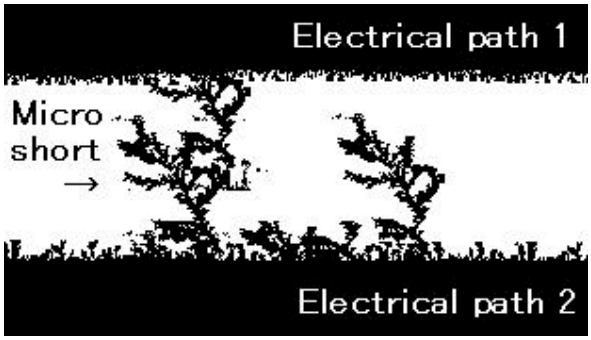

Figure 3 - Occurrence of a Micro Short

Although supplying a high electrical voltage between the isolated patterns can cut the microshorts permanently, such procedure is considered not appropriate for high-speed HDI substrates. This is because the blown microshorts still introduce various signal distortions in a high-speed transmission line. The disconnected microshorts readily become the sources of signal reflections and crosstalks. Figure 4 illustrates a simulated waveform obtained from a pair of transmission lines with a disconnected microshot. Presence of reflection point at the broken microshot in this circuit seriously affects on the operation of high speed digital devices associated in the circuit.

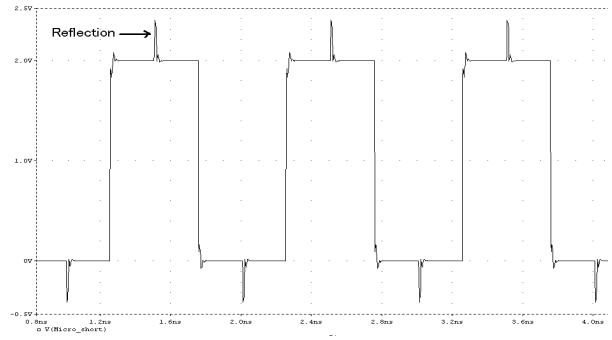

Figure 4 - Simulated Waveform of Reflection Due to a Micro Short

To prevent from undesirable reflection effects, it is required to detect the microshort existence, and failed substrates should be rejected to proceed further processing.

C. Erratic Shorts

The insulation characteristics of the material between two electrical paths may deteriorate under a high voltage electrical pressure even though it has excellent isolation at low voltage conditions. This phenomenon of shorted patterns under a high voltage is called "erratic" shorts.

Failure Detection Techniques for HDI Substrates

1. Incomplete vias

Since the resistance increment due to an incomplete via is much less than 1Ω, typical measurement technique of using two wires to simultaneously measure voltage and current is no longer applicable. A popular approach used to detect an incomplete via is the four-terminal resistance measurement method.

Figure 5 represents the principle of the four-terminal resistance measurement technique. The measurement circuit applies a constant current I to an unknown load resistance Ro and a voltmeter exactly measures the voltage E across it. Since the unit includes individual terminals for each of the current drive Hc, current sense Lc, high-side voltage sense Hp and low-side voltage sense Lp, the influences of contact and wire resistances, r1 through r4, can be neglected. Hence the input impedance of voltmeter is typically more than 100kΩ, and the wiring and contact resistances of the probes Hp and Lp are in several ohms range, the current flow through r3 or r4 is extremely small,

$$Ir3 = Ir4 \approx 0 \quad (1)$$

and the voltage across r3 and r4 are

$$Vr3 \approx 0 \quad (2)$$

$$Vr4 \approx 0. \quad (3)$$

Therefore, the voltage Eo across the unknown resistance can be expressed as

$$Eo \approx E \quad (4)$$

The constant current I that flows through r1 and r2, is equals the current through Ro,

$$I_{r1} = I_{r2} = I_{Ro} = I \quad (5)$$

Thus, the unknown resistance Ro can be accurately obtained from the measured values as

$$Ro = \frac{E}{I} \quad (6)$$

Please note that equation (6) does not include any wiring or contact resistance terms. Therefore, if the measurement resolutions of current and voltage are high enough, this technique can be successfully applied to detect subtle changes in pattern resistances, including the case of partially filled microvias.

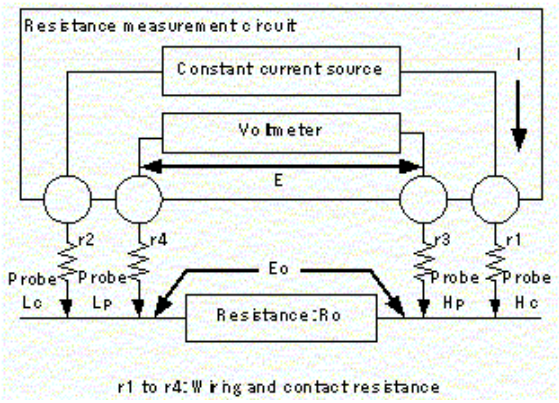

Figure 5 Four-Terminal Resistance Measurement

For that to happen, a miniature four-terminal probe is essential to characterize microvias because these probes must land on small pads and bumps. Figure 6 shows a four-terminal probe for flying probe tester realized by HIOKI E.E. Corporation of Japan. The probe is structured to accommodate both potential measurement probes (Hp and Lp) and current source probe (Hc and Lc) as close as possible. With this structure, minimum pitch of 100 micron in x direction and 150 micron in y direction are measurable. In addition to small pitch sizes, this probe is also designed to hit soft pad materials with minimal indentation witness marks.

Figure 6 – Four-Terminal Probe

2. Microshorts and Erratic Shorts

To detect both microshots and erratic shorts, the electrical test procedure must be carefully tailored. If high voltage isolation test is performed prior to low voltage test on a product substrate, microshorts are likely to be broken, and that makes one impossible to detect them with subsequent electrical test procedure. Figure 7 is the proposed electrical testing routine designed to fulfill the requirement for finding both microshorts and erratic layer shorts. In this model the low voltage test is first applied so that the microshoted and physically shorted PWBs can be rejected in the first place.

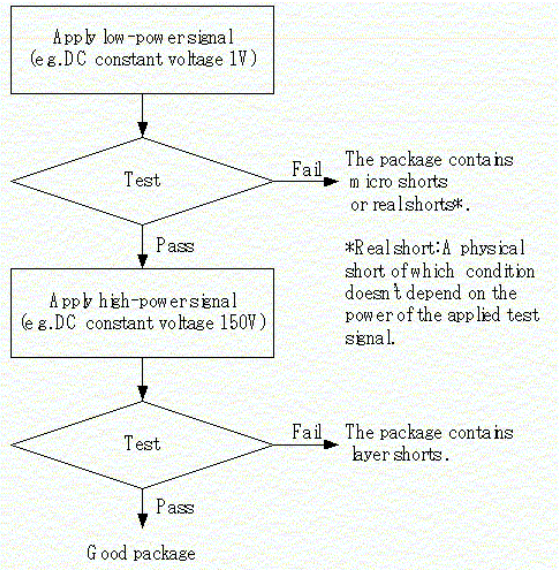

Figure 7 – Typical Testing Sequence for Micro Shorts and Layer Shorts Detection

Suggested Test Strategies for HDI PWB Production

In Figure 8, a practical example of test plan used in a FC-PGA production environment is provided. At the phase of prototype evaluation and small volume pilot production, high speed flying probe testers can be installed to meet electrical test requirements.

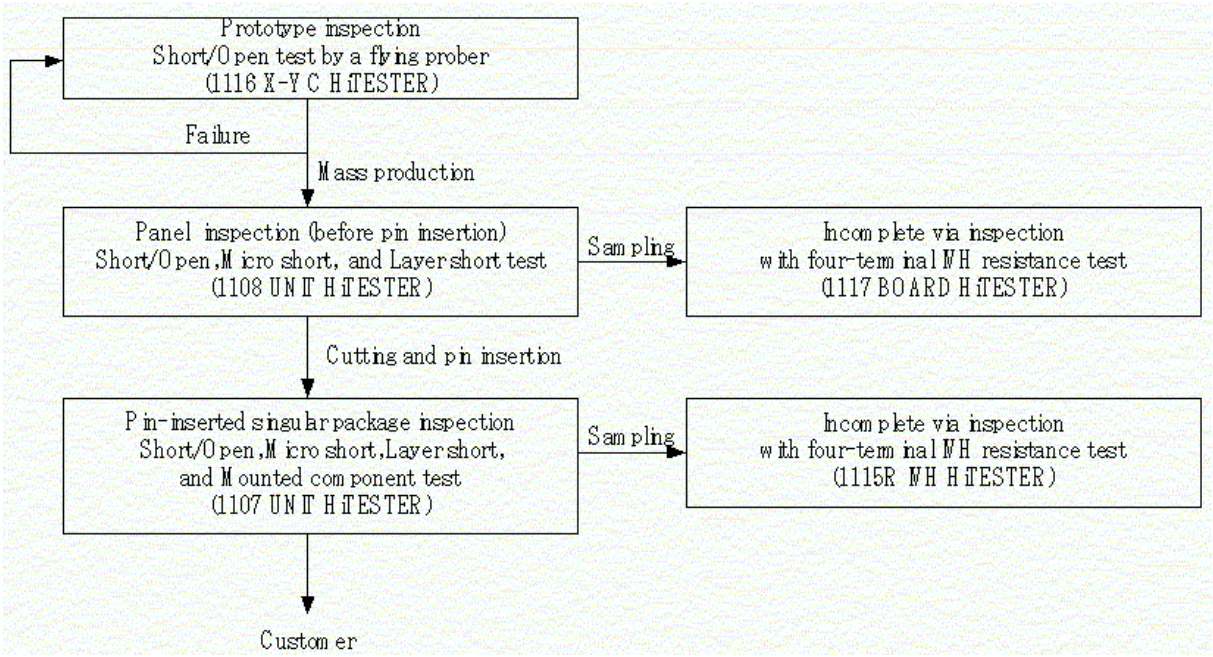

Figure 8 – Example of a Configuration for FC-PGA Inspection

For the mass production phase, a panel electrical tester should be employed prior to singulating and pin insertion processes to find out various defects like short/open, microshorts, and erratic layer shorts on all of the panels. This intermediate test is crucial because of its costs reduction effect. Finding bad parts at this point will prevent further process such as inserting pins into defective parts. Only the good parts are forwarded to the processes of singulated substrates.

Incomplete via inspection can be carried out by four-terminal IVH true resistance test systems. At the prototyping and pilot production phases, most of the panels or packages should be tested by the true resistance tester. The sampling test approach can be used once the manufacturing process stabilizes, keeping in mind that the sampling rate is directly related to the quality assurance issues of the manufacturing process.

Impedance Measurement with TDR System

Characteristic impedance measurement with TDR is becoming a mandatory test routine nowadays for the applications of CPU substrates with clock frequencies over 1GHz. In this section, the requirement for having uniform characteristic impedance and TDR principle for measuring the impedance will be briefly discussed.

If the pattern width, thickness, dielectric constant of a substrate material, and the operating temperature vary, high frequency response of the package will drastically change. The signal propagating through the transmission line will reflect at any point where there in impedance mismatch and the reflection in turn affects signal transmission required for processor operations. Therefore, it is crucial to control pattern width, thickness, and dielectric constant so that characteristic impedance of the substrate is uniform in accordance with the requirements of CPU specifications.

Figure 9 shows a sample transmission line with non-uniform characteristic impedance. This transmission line has nominal impedance of 50-ohms, but it also has narrow line widths with impedance of 70 ohms and a wide pattern of 30 ohms impedance.

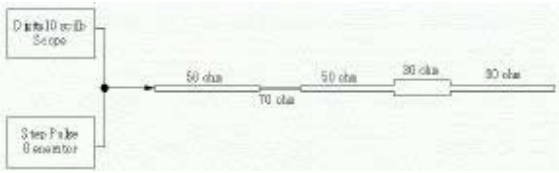

Figure 9 – Example of a Configuration of TDR and a Non-Uniform Transmission Line

To measure the characteristic impedance, an electrical pulse is applied by using a pulse generator from one end of the transmission line and the response waveform is recorded. Figure10 shows actual captured waveform for this example.

Once the waveform is obtained, the characteristic impedance and the locations of non-uniformed impedances can be calculated as shown the result in Figure 11.

In this way, the quality of a transmission line on a package can be evaluated by using TDR measurement.

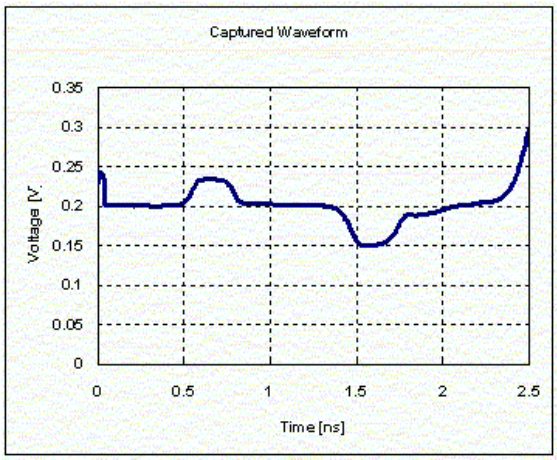

Figure 10 - Captured Waveform

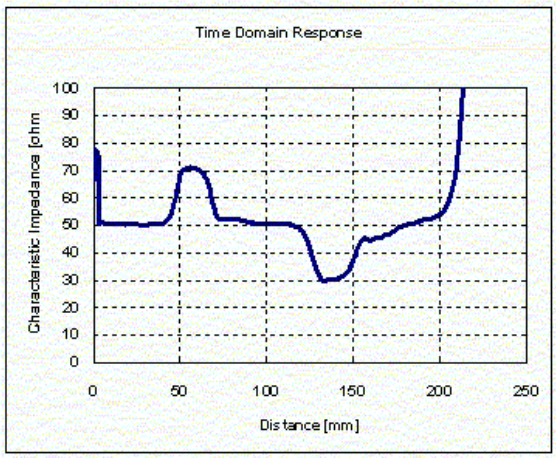

Figure 11 – Calculated Characteristic Impedance

Conclusion

We have discussed common failure modes of HDI packages and the solutions for detecting these failures are also described in this report. Higher clock frequencies of digital circuit systems brought up new technical challenges to the PWB manufacturers. Many problems in the substrates become evident only after the chips are mounted, packed and tested for operation. Our effort is in this paper to suggest an earlier detection of such failures by fully exploiting the available precision electrical measurement techniques. Although the evaluation techniques described here may not cover all failure modes of HDI substrates, the authors expect that these techniques will help avoid most of the problems originated in bare board substrates.

References

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